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Single-phase current source converter with high reliability and high power density

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Abstract: For single-phase current source converter (SCSC), at least one upper device and one lower device have to be gated on and maintained at any time. Otherwise, an open-circuit of the DC-link current would occur and destroy the devices. In addition, a bulky DC-link inductor is usually required to obtain a smooth DC-link current. To address these issues, this study proposes a novel SCSC with high reliability and high-power density. In the proposed circuit, even all the switches are turned on or turned off simultaneously, neither short-circuit nor open-circuit will happen. The inductance in DC-side is reduced significantly byadopting the active power decoupling technique. First, the operation principle of the proposed converter is introduced in detail. Then, a closed-loop control method is presented to regulate the DC-link current, maintain the DC component of the decoupling capacitor voltage, and achieve sinusoidal grid current. Besides, the parameter design of the circuit and controller is investigated. Moreover, the efficiency comparison between the proposed and other SCSCs is carried out. Finally, the effectiveness of the proposed topology is verified by the experimental results.

1 Introduction

The pulse-width modulated current source converters (CSCs) possess many attractive features, such as reliable short-circuit protection, high reliability (no electrolytic capacitors) and limited inrush current [1–3]. In recent years, they have received considerable attention and have been good candidates for applications in photovoltaic power system [2, 4], data center system [5], fuel cell power supply system [6], megawatt-motor-drive [7] and so on. In CSCs, the DC-link inductor is crucial to smooth the DC-link current [8]. In a symmetric three-phase system, the DC-link inductor can be small as it only needs to filter the switching harmonics [3]. However, for single-phase system, a bulky inductor is usually required to buffer the ripple power at twice the grid frequency and limit the DC-link current ripple in the allowable range. This method of achieving smooth DC-link current is called a passive power decoupling method. In practice, it is unacceptable because the bulky inductor degrades the power density and dynamic response capability significantly [9–11].

To address this issue, the active power decoupling method has attracted increasing research interests [11, 12]. Its basic idea is to add a small capacitor to buffer the low-frequency ripple power by allowing a large voltage fluctuation. The literature [11, 12] give a comprehensive review of the developed decoupling circuits, which are divided into ac-side and dc-side decoupling solutions according to the locations of the decoupling capacitor. For the ac-side decoupling method, in [12–17], an extra switching bridge arm and a decoupling capacitor are added. In addition, the decoupling capacitor is connected between the added and the original switching bridge arms. In [18], a switch and a diode are added to each switching bridge arm. Then, there are two electrical ports with one being connected to the ac filter and the other connected to the decoupling capacitor. For the above-mentioned ac-side decoupling methods, two original switches are shared and play the role of rectification/inversion and power decoupling. For the dc-side decoupling, in [19, 20] a simplified H bridge circuit is inserted into the dc rail to buffer the ripple power. The highlight is that the decoupling part and the original rectification/inversion part will not interfere with each other, which makes the controller design easier. To reduce the number of switches, the switch-multiplexed versions are proposed in [21, 22]. The converter reduces semiconductor devices and passive components, which is beneficial for saving cost and increasing power density. As the research continues, more and more other functions, such as multi-level inversion [23], power factor correction (PFC) [24], voltage boost-up [25, 26] are merged into the decoupling circuits.

All above-mentioned single-phase CSC (SCSCs) have a common problem that the open-circuit must be avoided to provide a path for the DC-link current. Otherwise, an open circuit of the DC-link current would occur and destroy the devices. The open-circuit caused by EMI noise's misgating-off is a major concern of the reliability. Moreover, the overlap time for safe current commutation is needed, which will cause waveform distortion. This issue can be overcome by adding a freewheel diode behind the converter [27]. However, the power factor is limited to be unity.

In this paper, a new SCSC with active power decoupling function is proposed. The proposed SCSC employs a small decoupling capacitor to buffer the ripple power and then the value and size of the DC-link inductor can be reduced significantly. The reliability is also improved because turning all the switches off at the same time is allowable, which avoids the open circuit risk. Moreover, compared to many other decoupling circuits for SCSCs [12, 18, 19], the proposed converter only adds one switch and two diodes, which means one semiconductor device is saved. In addition, the proposed SCSC can produce reactive power.

The remaining of the paper is organised as follows: Section 2 introduces the topology derivation and operation principles of the proposed SCSC. In Section 3, the modelling and control scheme for the proposed topology is demonstrated. In Section 4, the parameter design for circuit and controller is presented. The power losses comparison with other SCSCs is provided in Section 5. In Section 6, the experimental results are illustrated, and finally, Section 7 summarises the major contributions and discusses future work.

2 Topology analysis

2.1 Circuit derivation

The SCSC in [19] is redrawn and shown in Fig. 1*a*. The simplified H bridge circuit is composed of switches S_5, S_6 and diodes D_5, D_6, which are used to buffer the low-frequency ripple power. As shown in Fig. 1*b*, by connecting the cathode end of the diode D_5 to the upper dc rail and then removing the redundancy (the switch S_6), the

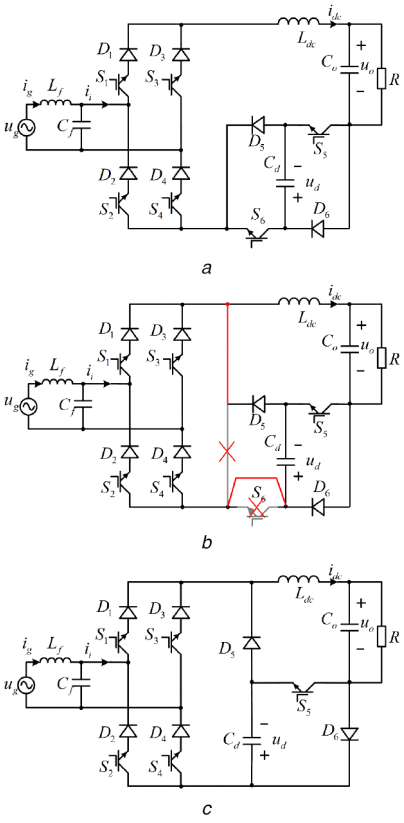

Fig. 1 *Topology structure derivation*
(a) Circuit proposed in [19], ***(b)*** Topological deformation process, ***(c)*** Proposed converter

proposed SCSC shown in Fig. 1*c* is derived. In addition to preserving the ripple power decoupling capacity, the proposed SCSC has some other merits. First, the cost is reduced for saving one switch. Second, each DC-link current path involves fewer semiconductor devices, especially when the zero vector is carried out (only two semiconductor devices are in the DC-link current path). Consequently, conduction power losses can be reduced remarkably. Third, even all the switches are turned on or turned off at the same time, neither short-circuit nor open-circuit will happen, which leads to a high reliability.

2.2 Switching states

The proposed topology has ten switching states, which are shown in Fig. 2. In the figure, the switching state combination ($S_1S_2S_3S_4S_5$) denotes the states of five active switches, where the logics 0 and 1 indicate the switch is on-state and off-state, respectively.

The switching states in Fig. 2 can be divided into four groups in terms of functionality.

Group I: Rectifying mode, including switching states 1 and 2. This group is used for synthesising input current. Also, the decoupling capacitor C_d is bypassed.

Group II: Decoupling mode, including switching states 3, 4 and 5. This group is to achieve ripple power absorbing/releasing. In switching state 3 the capacitor C_d is charged so that the excess power is absorbed. Conversely, the capacitor C_d is discharged and the insufficient power is supplemented with switching states 4 and 5. The power grid is disconnected with the decoupling circuit.

Group III: Freewheeling mode, including switching states 6, 7 and 8. This group provides the freewheeling path for the DC-link current i_{dc}. In practice, switching state 6 is adopted to achieve the least power losses.

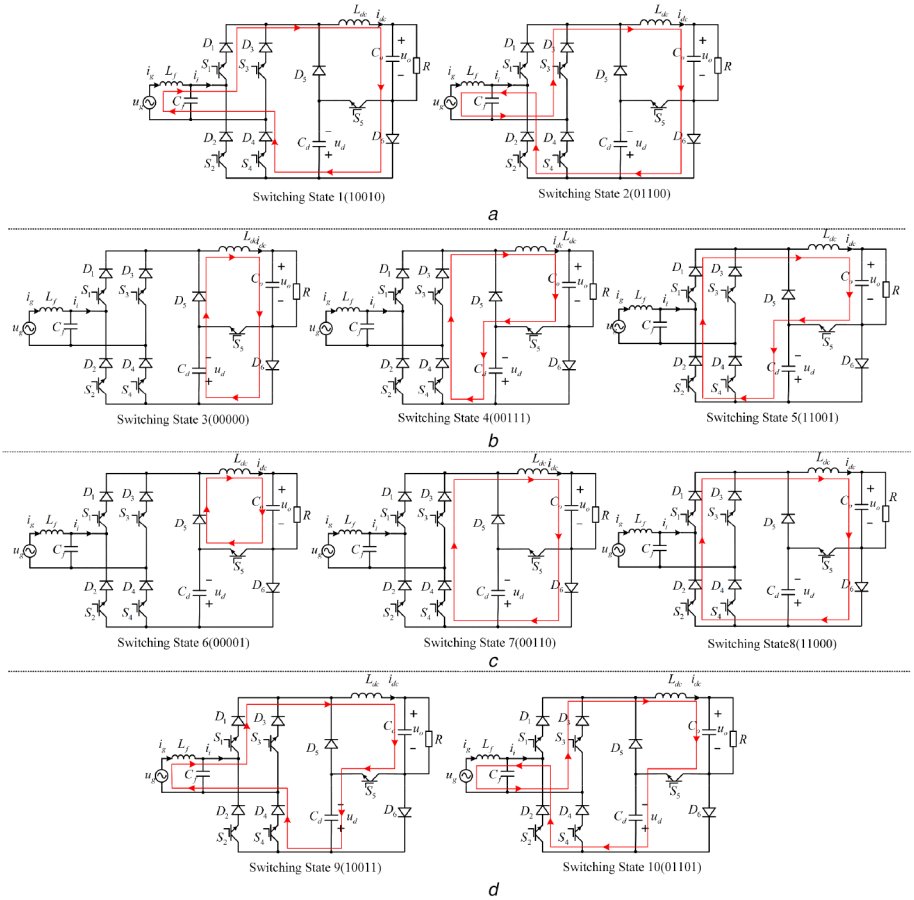

Fig. 2 *Switching states of the proposed topology*
(a) Group I, ***(b)*** Group II, ***(c)*** Group III, ***(d)*** Group IV

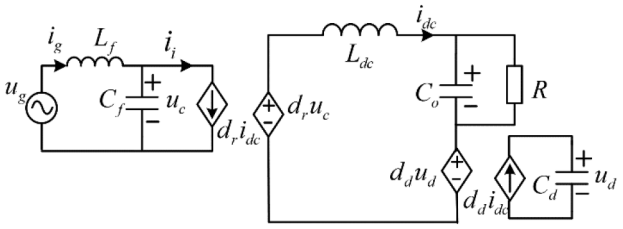

Fig. 3 *Equivalent circuit of the proposed topology*

Group IV: Rectifying and decoupling mode, including switching states 9 and 10. This group is used to achieve both the input current synthesis and the ripple power buffering. It should be noted that the capacitor can only be discharged with these switching states.

2.3 Operation principle

Assuming the grid voltage u_g and current i_g are expressed as

$$u_g = V\cos(\omega t) \tag{1}$$

$$i_g = I\cos(\omega t + \varphi) \tag{2}$$

where V and I are the amplitudes of grid voltage and current, respectively, ω is the angular frequency and φ is the displacement angle.

Then, the instantaneous power p_{ac} of the grid can be derived as

$$p_{ac} = u_g i_g = \underbrace{VI\cos\varphi/2}_{\bar{P}} + \underbrace{VI\cos(2\omega t + \varphi)/2}_{\tilde{P}} \tag{3}$$

It is obvious that p_{ac} consists of the constant power $\bar{P}$ and the ripple power $\tilde{P}$ at twice the grid frequency. Ignoring the system power losses, the load power P_o equals to $\bar{P}$.

If $\tilde{P}$ is completely buffered by the decoupling capacitor C_d, the voltage and current of C_d can be deduced according to the power balance [18]

$$u_d = \sqrt{\bar{u}_d^2 + \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \tag{4}$$

$$i_d = \frac{VI\cos(2\omega t + \varphi)}{2\sqrt{\bar{u}_d^2 + (VI\sin(2\omega t + \varphi)/2\omega C_d)}} \tag{5}$$

where $\bar{u}_d$ is the dc component of u_d.

The basic mechanism is as follows: when $p_{ac} \geq P_o$, the ripple power is absorbed by C_d, its current i_d is positive and voltage u_d is increasing; when $p_{ac} < P_o$, the energy is released from C_d, its current i_d is negative and voltage u_d is decreasing.

3 Modelling and control

3.1 Modelling

The average model of the proposed topology is expressed as

$$L_f \frac{di_g}{dt} = u_g - u_c \tag{6}$$

$$C_f \frac{du_c}{dt} = i_g - i_i \tag{7}$$

$$L_{dc} \frac{di_{dc}}{dt} = d_r u_c - u_s - u_o \tag{8}$$

$$C_d \frac{du_d}{dt} = i_d \tag{9}$$

$$C_o \frac{du_o}{dt} = i_{dc} - \frac{u_o}{R} \tag{10}$$

$$i_i = d_r i_{dc} \tag{11}$$

$$i_d = d_d i_{dc} \tag{12}$$

$$u_s = d_d u_d \tag{13}$$

where u_c is the terminal voltage of capacitor C_f, u_o is the voltage of load, u_s is the equivalent voltage provided by C_d, i_i is the input current of the converter, i_{dc} is the DC current flowing through inductor L_{dc}, d_r is used to control the input current and d_d is used to control the ripple power. In addition, d_r, d_d should be subjected to $-1 \leq d_d, d_r \leq 1$ condition. The equivalent circuit of the proposed topology is illustrated in Fig. 3.

In this paper, only the switching states 1, 2, 3, 4 and 6 are adopted to accomplish the goals of input current synthesis and ripple power mitigation. By using these switching states, the rectifying and decoupling are performed separately.

Assume d_j ($j = 1, 2, 3, 4, 6$) is the duty ratio of the switching state j, there is

$$d_1 + d_2 + d_3 + d_4 + d_6 = 1 \left(0 \leq d_j \leq 1\right) \tag{14}$$

Then d_r and d_d can be expressed as

$$\begin{cases} d_r = d_1 - d_2 \\ d_d = d_3 - d_4 \end{cases} \tag{15}$$

Combining (6)–(15), the duty ratios d_j in steady-state can be obtained as follows:

$$d_r = i_{iref}/i_{dc}, d_d = u_{sref}/u_d \tag{16}$$

$$\begin{cases} d_1 = \begin{cases} i_{iref}/i_{dc}, & i_{iref} > 0 \\ 0, & i_{iref} \leq 0 \end{cases} \quad d_2 = \begin{cases} 0, & i_{iref} > 0 \\ i_{iref}/i_{dc}, & i_{iref} \leq 0 \end{cases} \\ d_3 = \begin{cases} u_{sref}/u_d, & u_{sref} > 0 \\ 0, & u_{sref} \leq 0 \end{cases} \quad d_4 = \begin{cases} 0, & u_{sref} > 0 \\ -u_{sref}/u_d, & u_{sref} \leq 0 \end{cases} \\ d_6 = 1 - \sum_{j=1}^{4} d_j \end{cases} \tag{17}$$

where i_{iref} and u_{sref} are the references of the control input variables.

Based on the above analysis, d_r and d_d in steady-state can be plotted as shown in Fig. 4*a*. Combining with (17), the switching sequences under different cases adopted in this paper are shown in Fig. 4*b*. As seen, one grid frequency cycle is divided into four sections. There are three switching states in each section, starting with the rectifying mode, then turning to the decoupling mode and ending with the freewheeling mode. According to (17) and Fig. 4, it is easy to implement the modulation of the proposed topology by the field-programmable gate array (FPGA).

3.2 Control strategy

The control objectives of the proposed topology are: (i) to keep constant DC-link current; (ii) to obtain sinusoidal input current; (iii) to maintain the dc component of u_d.

According to (8)–(12), the control inputs are d_d and d_r, the state variables are i_g, i_{dc} and u_d. Both d_d and d_r can regulate the DC-link current i_{dc}. By adopting the proposed control scheme in [21], d_d is used to control the DC-link current and d_r is used to implement PFC as well as keeping the dc component of u_d as a constant. The overall control diagram is shown in Fig. 5.

3.2.1 DC-link current control: According to (8) and (11), the equivalent voltage provided by C_d can be obtained as follows:

$$u_{sref} = -G_i(s)(i_{dcref} - i_{dc}) - u_o + \frac{i_{iref}}{i_{dc}} u_c \tag{18}$$

where $G_i(s) = K_{pi} + K_{ii}/s$ and $u_o = i_{dc}R$.

Then, the dynamic of the inductor current is rewritten as

$$L_{dc}\frac{di_{dc}}{dt} = G_i(s)(i_{dcref} - i_{dc}) \tag{19}$$

It is clear that (19) is asymptotically stable under $K_{pi} > 0$ and $K_{ii} > 0$.

3.2.2 Capacitor voltage control: Multiplying u_d on both sides of (9), and combining (12), (16) with u_s in steady-state ($u_s = -u_o + (i_i/i_{dc})u_c$), we can obtain

$$\frac{1}{2}C_d\frac{du_d^2}{dt} = i_i u_c - P_o \tag{20}$$

where $P_o = u_o i_{dc}$ is the load power.

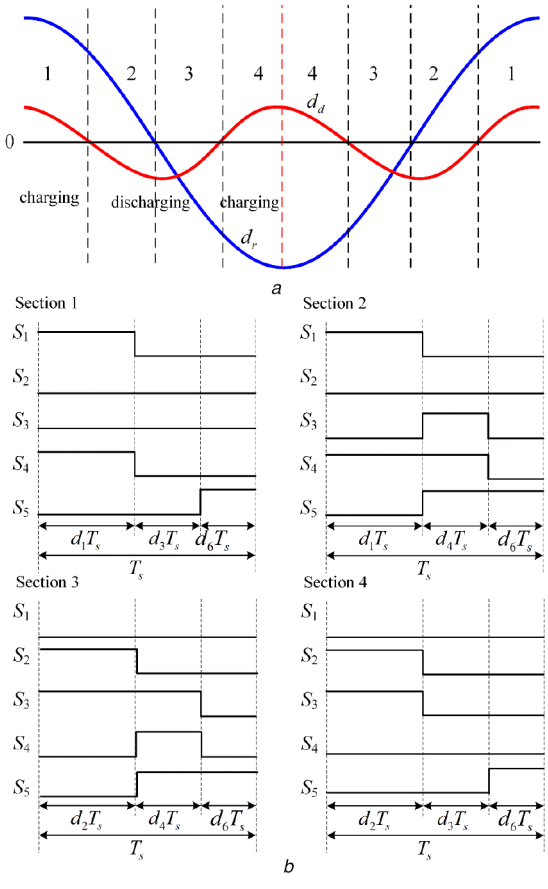

Fig. 4 *PWM signals under different cases*
(a) Schematic diagram of d_r and d_d in steady-state, ***(b)*** PWM signals for five active switches

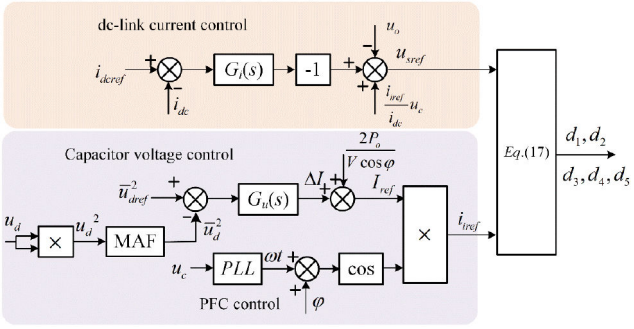

Fig. 5 *Control scheme of the proposed topology*

Ignoring the effects of the input filter, $u_c$and i_i could be approximated equal to u_g and i_g, respectively. Then, (20) can be rewritten as

$$\frac{1}{2}C_d\frac{du_d^2}{dt} = \frac{VI}{2}\cos\varphi + \frac{VI}{2}\cos(2\omega t + \varphi) - P_o \tag{21}$$

Notice that the periodic perturbation has zero mean, so the averaged equation becomes

$$C_d\frac{d\overline{u_d^2}}{dt} = VI\cos\varphi - 2P_o \tag{22}$$

where $\overline{u_d^2} = 1/T\int_0^T u_d^2 dt$, and it can be obtained by the moving average filter. In (4), it can be found that $\overline{u_d^2} = \bar{u}_d^2$.

Based on (22), the amplitude of grid current reference I_{ref} is designed as

$$I_{ref} = G_u(s)\left(\bar{u}_{dref}^2 - \bar{u}_d^2\right) + \frac{2P_o}{V\cos\varphi} \tag{23}$$

where $G_i(s) = K_{pu} + K_{iu}/s$.

Substituting (23) into (22), it leads to

$$C_d\frac{d\bar{u}_d^2}{dt} = G_u(s)\left(\bar{u}_{dref}^2 - \bar{u}_d^2\right)\cdot V\cos\varphi \tag{24}$$

As seen, (24) is asymptotically stable under $K_{pu} > 0$ and $K_{iu} > 0$.

To achieve PFC, the phase information is obtained by the phase-locking loop of u_c. Thus, the reference of the input current is expressed as

$$i_{iref} = I_{ref}\cos(\omega t + \varphi) \tag{25}$$

4 Parameter design

4.1 Selection of $\bar{u}_d$ and C_d

In this section, the values of $\bar{u}_d$ and C_d are designed. According to (15), the duty ratios d_d and d_r in the steady state can be further expressed as

$$d_r = I\cos(\omega t + \varphi)/i_{dc} \tag{26}$$

$$d_d = u_o\cos(2\omega t + \varphi)/u_d \tag{27}$$

To ensure normal operation, the following constraints should be satisfied: (i) $u_d > 0$; (ii) $|u_g|$ $\text{sign}(p_{ac}) + u_d > 0$; and (iii) $|d_d| + |d_r| \le 1$. Thus, we can obtain

$$\bar{u}_d \ge \sqrt{VI/2\omega C_d} \tag{28}$$

$$\begin{cases} u_d > -|u_g|, \text{whencos}\,\varphi \ge \cos(2\omega t + \varphi) \\ u_d > |u_g|, \text{whencos}\,\varphi < \cos(2\omega t + \varphi) \end{cases} \tag{29}$$

$$\frac{|u_o\cos(2\omega t + \varphi)|}{\sqrt{\bar{u}_d^2 + (VI\sin(2\omega t + \varphi)/2\omega C_d)}} + \frac{|I\cos(\omega t + \varphi)|}{I_{dc}} \le 1 \tag{30}$$

Neglecting the power losses u_o can be replaced by $VI/2I_{dc}$. The modulation index is defined as $m = I/I_{dc}$. Then, (30) can also be expressed as

$$\bar{u}_d \ge \sqrt{\frac{m^2V^2\cos^2(2\omega t + \varphi)}{4(1 - m|\cos(\omega t + \varphi)|)^2} - \frac{VI\sin(2\omega t + \varphi)}{2\omega C_d}} \tag{31}$$

Besides, the maximum voltage stress on switches should be considered, i.e. that

$$\sqrt{\bar{u}_{\mathrm{d}}^2+\frac{VI_{\mathrm{m}}}{2\omega C_{\mathrm{d}}}}\le u_{\mathrm{p}} \tag{32}$$

where u_{p} denotes as the maximum permissible voltage of semiconductor switches and I_{m} is the maximum grid current.

Assuming that the converter operates in unity power factor in following parameter design, as observed, (29) is strictly satisfied. Then, based on inequalities (28), (31) and (32), the range of $\bar{u}_{\mathrm{d}}$ is

$$\bar{u}_{\mathrm{dmin}}\le\bar{u}_{\mathrm{d}}\le\bar{u}_{\mathrm{dmax}} \tag{33}$$

where

(see (34))

(see (35))

By substituting the parameters adopted in this paper (in Table 1) into (33), the feasible range of $\bar{u}_{\mathrm{d}}$ is depicted in Fig. 6. It is found that $\bar{u}_{\mathrm{dmin}}\le\bar{u}_{\mathrm{dmax}}$ is always established at any instant. To reduce the power losses and leave some margin, $\bar{u}_{\mathrm{d}}$ is chosen to be slightly higher than $\bar{u}_{\mathrm{dmin}}$. It is worth noting that increasing C_{d} will decrease $\bar{u}_{\mathrm{d}}$. However, if C_d is beyond a certain value, the reduction is not obvious. In this paper, C_d is selected to 60 μF and $\bar{u}_{\mathrm{d}}$ is set to 250 V owing to the trade-off between power losses and system cost.

4.2 Selection of L_{dc}

According to Fig. 6, the current ripple of DC-link inductor can be calculated as

$$\Delta I_{\mathrm{dc}}=\begin{cases}\dfrac{(d_{\mathrm{r}}u_{\mathrm{g}}-|d_{\mathrm{r}}|u_{\mathrm{o}})}{f_{\mathrm{s}}L_{\mathrm{dc}}}, \text{when in Section1.4}\\ \dfrac{(1-|d_{\mathrm{r}}|-|d_{\mathrm{d}}|)u_{\mathrm{o}}}{f_{\mathrm{s}}L_{\mathrm{dc}}}, \text{when in Section2.3 and } |u_{\mathrm{g}}|\ge u_{\mathrm{o}}\\ \dfrac{|d_{\mathrm{d}}|(u_{\mathrm{d}}-u_{\mathrm{o}})}{f_{\mathrm{s}}L_{\mathrm{dc}}}, \text{when in Section2.3 and } |u_{\mathrm{g}}|<u_{\mathrm{o}}\end{cases} \tag{36}$$

where f_{s} is the switching frequency.

Further, the limit of L_{dc} is resolved as follows:

$$L_{\mathrm{dc}}\ge\max_{t\in(0,\frac{2\pi}{\omega})}\left(\frac{\Delta I_{\mathrm{dc}}}{\delta_i I_{\mathrm{dc}} f_{\mathrm{s}}}\right) \tag{37}$$

where δ_i is the current ripple index.

Thus, based on (37) and other parameters in Table 1, the inductance is selected as 5 mH while δ_{i} is chosen to 0.15.

4.3 Input filter design

The input filter influences the system size and grid current performance, so the careful design is needed. The first step is to determine the capacitance of the filter capacitor. Based on the constraints of the capacitor voltage ripple and the reactive current, the limits of the capacitance is as follows:

$$\frac{I_{\mathrm{dc}}}{4f_{\mathrm{s}}\delta_{\mathrm{v}}V}\le C_{\mathrm{f}}\le\frac{Q_{\mathrm{s}}}{\omega V^2} \tag{38}$$

where δ_{v} is the voltage ripple index, Q_{s} is the reactive power (depending on the input power factor requirement).

The next step is to choose an inductance of the input inductor. Assume the cut-off frequency of the input filter is f_{c} ($f_{\mathrm{c}}\in(0.1-0.5)f_{\mathrm{s}}$), then

Table 1 Parameters in the experiments

Parameters	Value
amplitude value of grid voltage (V)	141 V
angular frequency of grid voltage (ω)	100 πrad/s
input filter inductor (L_{f})	0.5 mH
input filter capacitor (C_{f})	10 μF
input passive damping resistor (R_{f})	27 Ω
decoupling capacitor (C_{d})	60 μF
inductor of DC-link (L_{dc})	5 mH
resistor of load (R)	4 Ω
output capacitor (C_{o})	10 μF
bandwidth ω_{n1}	800 πrad/s
bandwidth ω_{n2}	40 πrad/s
average capacitor voltage$\bar{u}_{\mathrm{dref}}$	250 V
control period (T_{s})	100 μs

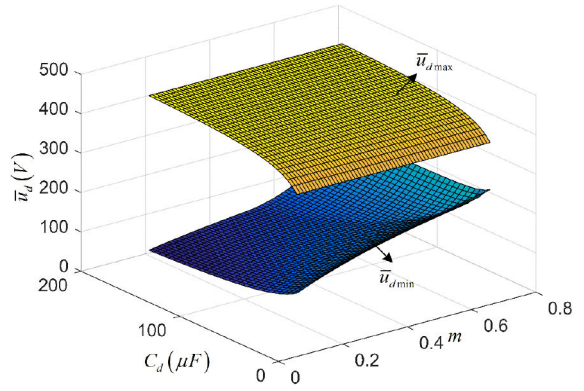

Fig. 6 *Schematic diagram of the feasible region of $\bar{u}_d$ and C_d*

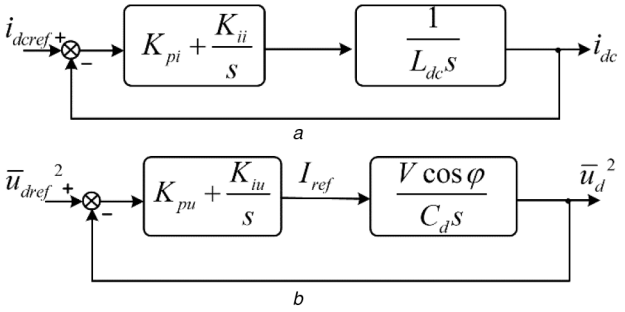

Fig. 7 *Diagram of the two control loops*
(a) DC-link current control loop, ***(b)*** Capacitor voltage control loop

$$L_{\mathrm{f}}=\frac{1}{4\pi^2 f_{\mathrm{c}}^2 C_{\mathrm{f}}} \tag{39}$$

Based on (38), (39), one of the input filter designs listed in Table 1 is selected.

4.4 Parameters design of controller

Based on (19), the DC-link current control loop can be derived as shown in Fig. 7*a*. Therefore, the closed-loop transfer function of DC-link current control loop is as follows:

$$\bar{u}_{\mathrm{dmin}}=\max\left(\sqrt{VI/2\omega C_{\mathrm{d}}},\max_{t\in(0,2\pi/\omega)}\left(\sqrt{\left(m^2V^2\cos^2(2\omega t+\varphi)/4(1-m|\cos(\omega t+\varphi)|)^2\right)}-(VI\sin(2\omega t+\varphi)/2\omega C_{\mathrm{d}})\right)\right), \tag{34}$$

$$\bar{u}_{\mathrm{dmax}}=\sqrt{u_{\mathrm{p}}^2-(VI_{\mathrm{m}}/2\omega C_{\mathrm{d}})}\,. \tag{35}$$

Table 2 Current stress analysis of proposed topology and other SCSCs

Topology	Component	I_{avg}, A	I^2_{rms}, A
proposed SCSC	S_1, D_1, S_2, D_2	$\frac{I}{\pi}$	$\frac{I_{dc}I}{\pi}$
	S_3, D_3, S_4, D_4	$\frac{I}{\pi}+\frac{\omega C_d}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$	$\frac{I_{dc}I}{\pi}+\frac{\omega C_d I_{dc}}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$
	S_5, D_5	$I_{dc}-\frac{2I}{\pi}-\frac{\omega C_d}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$	$I_{dc}^2-\frac{2I_{dc}I}{\pi}-\frac{\omega C_d I_{dc}}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$
	D_6	$\frac{2I}{\pi}+\frac{\omega C_d}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$	$\frac{2I_{dc}I}{\pi}+\frac{\omega C_d I_{dc}}{\pi}\left(\sqrt{\tilde{u}_d^2+\frac{VI}{2\omega C_d}}-\sqrt{\tilde{u}_d^2-\frac{VI}{2\omega C_d}}\right)$
conventional SCSC	S_1, D_1, S_2, D_2	$\frac{I}{\pi}$	$\frac{I_{dc}I}{\pi}$
	S_3, D_3, S_4, D_4	$\frac{I_{dc}}{2}$	$\frac{I_{dc}^2}{2}$
topology in Fig. 1*a*	S_1, D_1, S_2, D_2	$\frac{I}{\pi}$	$\frac{I_{dc}I}{\pi}$
	S_3, D_3, S_4, D_4	$\frac{I_{dc}}{2}$	$\frac{I_{dc}^2}{2}$
	S_5, D_6	$\frac{I_{dc}}{2}$	$\frac{I_{dc}^2}{2}$
	S_6, D_5	$\frac{I_{dc}}{2}$	$\frac{I_{dc}^2}{2}$

$$G_i(s)=\frac{K_{pi}s+K_{ii}}{L_{dc}s^2+K_{pi}s+K_{ii}} \tag{40}$$

To simplify the design, setting (40) as a standard second-order oscillation element, then, K_{pi} and K_{ii} can be designed as

$$K_{pi}=2\eta L_{dc}\omega_{n1}, K_{ii}=L_{dc}\omega_{n1}^2 \tag{41}$$

where ω_{n1} represents the bandwidth of DC-link current control loop, η is the damping factor and it is set to 0.707 in general. A large bandwidth (ω_{n1}= 800 πrad/s) is selected to regulate DC-link current tightly.

Based on (24), the capacitor voltage control loop is shown in Fig. 7*b*. The closed-loop transfer function can be expressed as

$$G_u(s)=\frac{K_{pu}s+K_{iu}}{C_d s^2/V\cos\varphi+K_{pu}s+K_{iu}} \tag{42}$$

According to the above tuning process, K_{pu} and K_{iu} are selected as

$$K_{pu}=2\eta C_d\omega_{n2}/V\cos\varphi, K_{ii}=C_d\omega_{n2}^2/V\cos\varphi \tag{43}$$

where ω_{n2} represents the bandwidth of the capacitor voltage control loop. In this study, to obtain high current quality, a lower bandwidth(ω_{n2}= 40 πrad/s) is applied to avoid changing the amplitude of the grid current fast.

5 Power loss analysis

The power losses of the converter mainly consist of the loss of semiconductor devices, capacitors and inductors. Usually, the power losses of semiconductor devices account for a large proportion, which includes conduction losses and switching losses. Both of them are related to the topology structure and the modulation strategy.

The conduction losses of IGBT can be calculated as follows [28]:

$$\begin{aligned}P_{c\_IGBT}&=\frac{1}{T}\int_0^T u_{CE}(i_s)\cdot i_s dt=\frac{1}{T}\int_0^T (u_{CE0}+r_{CE}i_s)\cdot i_s dt\\&=I_{Savg}u_{CE0}+I_{Srms}^2 r_{CE}\end{aligned} \tag{44}$$

where u_{CE} is the saturation voltage across the IGBT for current i_s, r_{CE} is the dynamic on-resistance of the IGBT, u_{CE0} is the forward voltage when the current is zero, I_{Savg} and I_{Srms} are the average and RMS currents of the IGBT, respectively.

Similarly, the conduction losses of the diode is deduced as

$$P_{c\_Diode}=I_{Davg}u_{F0}+I_{Drms}^2 r_F \tag{45}$$

where I_{Davg} and I_{Drms} are the average and RMS currents of the diode, respectively, u_{F0} is the forward voltage when the current is zero, and r_F is the dynamic on-resistance of the diode.

To calculate the switching losses, it is supposed that the switching loss is proportional to the switching voltage and the conducting current in a switching period [28]. Thus, the turn-on loss, turn-off loss and diode reverse recovery loss are represented as follows:

$$\begin{cases}E_{on}=k_{on}u_s i_s\\E_{off}=k_{off}u_s i_s\\E_{rr}=k_{rr}u_s i_s\end{cases} \tag{46}$$

where the coefficients k_{on}, k_{off} and k_{rr} are obtained from datasheets or experiments, u_s and i_s are the voltage across the switch in off-state and the current through the switch in on-state.

Then, the average switching energy of IGBT in the proposed topology is calculated as

$$\bar{E}_S=\frac{1}{T}\int_0^T E_S dt=\frac{k_{on}+k_{off}}{T}\int_0^T u_s i_s dt \tag{47}$$

Thus, the average switching losses of the IGBT is calculated as

$$P_{S\_IGBT}=f_s\bar{E}_S \tag{48}$$

The average switching losses of the diode are written as

$$P_{S\_Diode}=f_s\bar{E}_D=\frac{f_s k_{rr}}{T}\int_0^T u_s i_s dt \tag{49}$$

For S_1–S_4 and D_1–D_4, the voltage stress u_s is equal to u_c. As for the semiconductor devices in the decoupling circuit (S_5, S_6, D_5, D_6), the voltage stress is much higher, which is equal to the decoupling capacitor voltage u_d.

Still assuming the converter works in unity power factor, the current stress of each semiconductor device in proposed SCSC, conventional SCSC and topology in Fig. 1*a* are summarised in Table 2.

It is clear that the power losses of S_1–S_4 and D_1–D_4 in conventional SCSC and topology in Fig. 1*a* are the same. By substituting the parameters in experiments into Table 2, and combining with (44)–(49), the power loss distribution is illustrated in Fig. 8*a*.

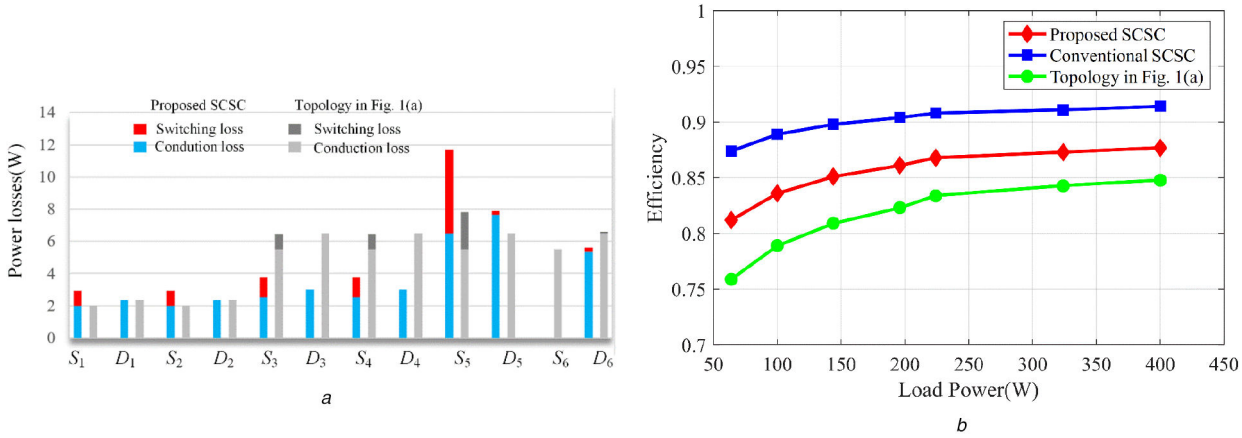

Fig. 8 *Power losses comparison under theoretical calculation*
(a) Loss distribution comparison under 400 W load power, ***(b)*** Efficiency comparison

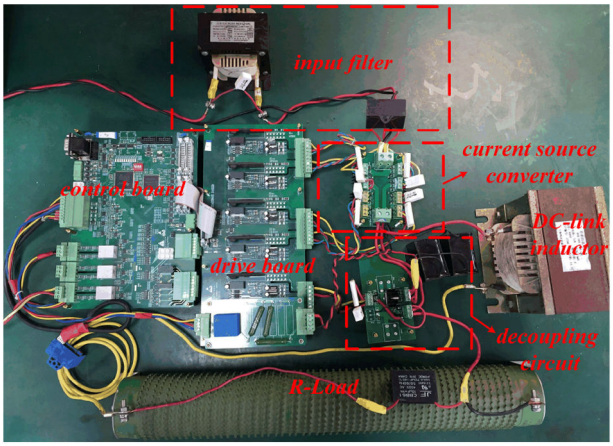

Fig. 9 *Experimental setup*

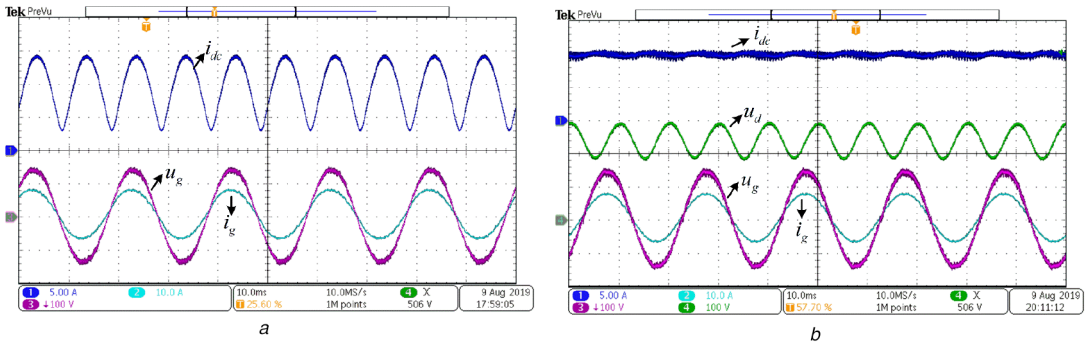

Fig. 10 *Experimental waveforms under Case I*
(a) Without decoupling circuit, ***(b)*** With decoupling circuit

The power losses of S_3, D_3, S_4 and D_4 in proposed topology are lower than those of conventional SCSC. As shown in Fig. 8*b*, the efficiency of the proposed converter is slightly lower than that of the conventional case due to the increased power losses of the decoupling circuit, but it is higher than that of topology in Fig. 1*a*.

6 Experimental results

An experimental prototype (shown in Fig. 9) is built to verify the proposed topology and the adopted control strategy. The schematic diagram of the proposed topology is shown in Fig. 1*c* and the related parameters are listed in Table 1. The IGBTs used in the main circuit are FGA40N65. The control strategy realised by the digital signal processor (DSP) TMS320F28335 and the FPGA EP2C8T144C8N. The DSP is responsible for implementing the proposed control strategy and transmitting the duty ratios to FPGA. The FPGA is used to generate the PWM signals.

The experiments are carried out in the following cases:

Case I: $i_{\text{dcref}} = 10$ A, $\varphi = 0$;
Case II: $i_{\text{dcref}} = 8$ A, $\varphi = \pm\pi/6$;
Case III: $i_{\text{dcref}} = 5$ A, $\varphi = 0$.

First, the feasibility of the designed decoupling circuit is tested by comparing the waveforms with/without decoupling circuit. When the proposed decoupling circuit is disabled, the converter works as a conventional SCSC and the resulting waveforms are shown in Fig. 10*a*. As illustrated, the DC-link current fluctuates with twice the grid frequency. When the decoupling circuit is activated, referring to Fig. 10*b*, the DC-link current is approximately constant. By importing the oscilloscope data into Matlab and then using the FFT tools, the THDs of grid current i_g under the proposed topology and no decoupling function topology are 2.82 and 4.31%, respectively. Both the THDs of i_g are <5%, which meet the requirements of standard IEC/EN 61000-3-2 Class A.

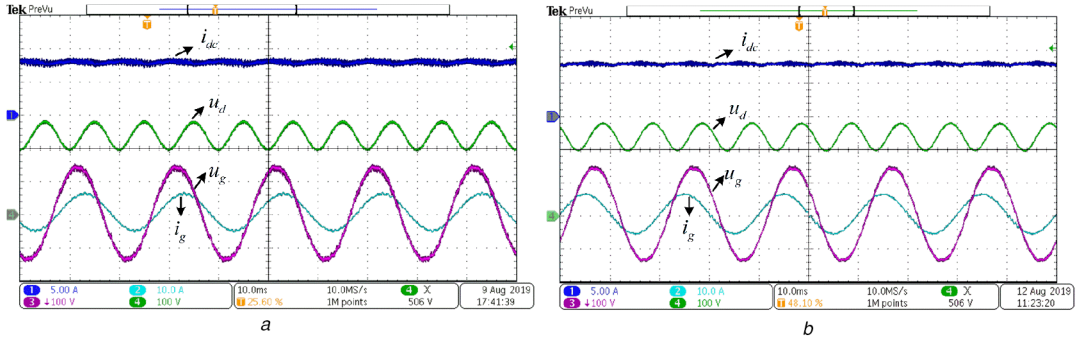

Fig. 11 *Experimental waveforms under Case II*
(a) $\varphi = -\pi/6$, ***(b)*** $\varphi = \pi/6$

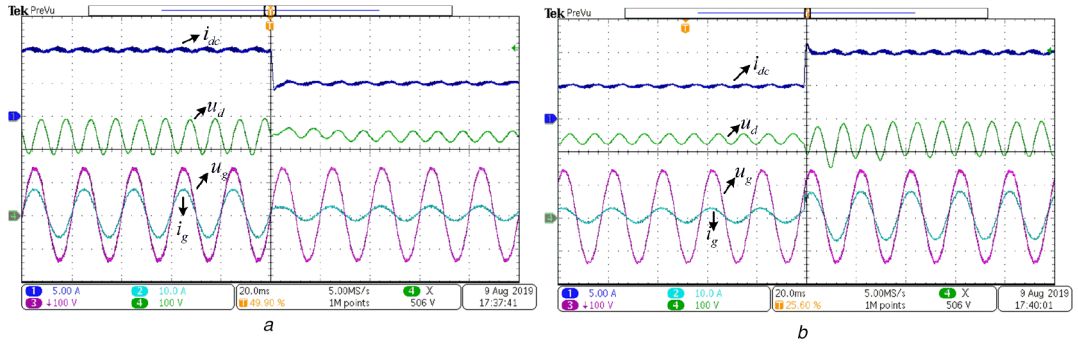

Fig. 12 *Experimental waveforms when DC-link current reference is changed abruptly*
(a) From Case I to Case III, ***(b)*** From Case III to Case I

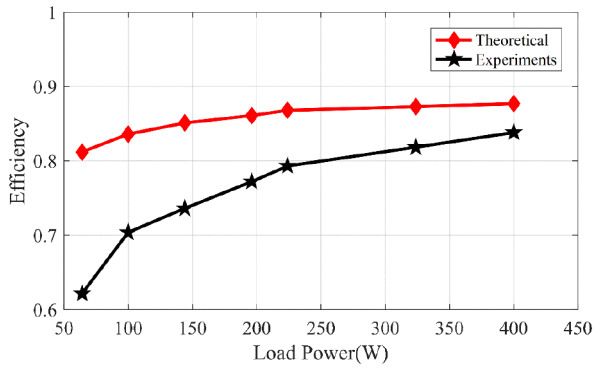

Fig. 13 *Efficiency of the proposed topology*

Second, different input power factors are performed. The experimental results when the input current lags and leads the input voltage $\pi/6$ are shown in Figs. 11*a* and *b*, respectively.

As seen, constant DC-link current and sinusoidal grid current are obtained. It can be concluded that the proposed topology has the capability to control the reactive power under the premise of ensuring the quality of grid and DC-link currents.

Third, the experiments with step references are conducted to show the dynamic response. As shown in Fig. 12*a*, when the DC-link current reference decreases from 10 to 5 A, the DC-link current tracks its reference immediately, the voltage of the decoupling capacitor becomes smaller. Fig. 12*b* shows the results of the DC-link current reference stepping up from 5 to 10 A. It is illustrated that there is no obvious distortion in the grid current in both cases. In addition, the dynamic response is fast and flat, which also verifies the rationality of parameter design.

Moreover, to verify the accuracy of the power losses modelling, the system efficiency is measured in the experiments as shown in Fig. 13. In addition, the nominal efficiency measured is 84.7%, which is a bit lower than the theoretical ones. The main reason is that the losses dissipated on input capacitors, PCB traces and current sensors are not considered in theoretical calculation. Also, the effect of those losses on system efficiency is more pronounced at low power.

Finally, Table 3 gives a comparison between different SCSCs with active power decoupling capability, it can be found that the count of the added semiconductor devices in the proposed topology is less than most other SCSCs. In addition, the control design for the proposed converter has low-complexity as the rectifying and decoupling circuit can work separately. Moreover, the highlight of the proposed topology is high reliability. It can be concluded that the proposed topology is a good candidate for decoupling the ripple power, especially for high reliability and high power density applications.

7 Conclusion

This paper presents a new SCSC topology with high reliability and high power density. In the proposed topology, the input will never be short-circuited and the output will never be left open, which leads to high reliability. Besides, a decoupling capacitor is utilised to buffer the ripple power. Thus, the power density is improved as the inductance of DC-link inductor is reduced greatly. A closed-loop control strategy is presented to achieve the fully power decoupling and high-quality grid current. Additionally, the guidance for parameter design is provided. As proved by experiments, the sinusoidal grid current and low-ripple DC-link current are achieved.

Table 3 Comparisons among different SCSCs with active power decoupling capability

Topologies	Power rating, W	Decoupling component (value)	Added semiconductor devices	Efficiency, %	Features
[16]	1000	1 capacitor (32 μF)	2 IGBTs + 2 diodes	—	decoupling capacitor also served as the input filter, increased control complexity
[17]	1500	1 capacitor (300 μF)	2 IGBTs + 2 diodes	—	horizon multiplexing, increased control complexity
[18]	1000	1 capacitor (50 μF)	2 IGBTs + 2 diodes	—	vertical multiplexing, increased control complexity
[19]	144	1 capacitor (91.8 μF)	2 IGBTs + 2 diodes	82	independent decoupling topology, flexible capacitor voltage range
[21]	217.5	1 capacitor (90 μF)	1 diode	78	no additional active switches, high-switching voltage stress
[22]	400	2 capacitors (90 μF)	2 diodes	90	no additional active switches, high efficiency
[24]	400	1 capacitor (100 μF)	2 MOSFETs + 1 diode	96.4	additional PFC function, decoupling capacitor voltage must be higher than the peak value of grid voltage, increased control complexity
proposed	400	1 capacitor (60 μF)	1 IGBT + 2 diodes	84.7	all switches turned on and turned off are allowable, high reliability

In the future, the study of the proposed SCSC will focus on improving the efficiency, reducing the cost with state observer, and improving performance with non-linear controllers.

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